Remarks

Claims 23-38 are presently pending. Claims 8-11, 21, and 22 are cancelled without prejudice. Claims 1-7, and 12-20 were previously cancelled without prejudice. Claims 23-38 have been added. Authorization to charge the $624.00 fee for additional claims is included in the fee transmittal form filed herewith.

Claims 8-11, 21, and 22, now cancelled without prejudice, were rejected. Applicants respectfully request reconsideration of the foregoing application in view of the foregoing amendments and the following remarks.

CLAIMS 23-30 ARE ALLOWABLE

Claim 23 is directed to "providing an output signal with a characteristic frequency that is a first integer, N, multiple of a characteristic frequency of an input signal", by "dividing the characteristic frequency of a[n] .... oscillator signal[s] by ...M, factor thereby providing the output signal with the characteristic frequency that is the first integer, N, multiple of the characteristic frequency of the input signal." Claims 27 is directed to a phase lock loop for "providing an output signal with a characteristic frequency that is a first integer, N, multiple of a characteristic frequency of an input signal" comprising "one or more divider

circuits for dividing the characteristic frequency of a[n] oscillator signal by the second integer, M, factor, thereby providing the output signal with the characteristic frequency that is the first integer, N, multiple of the characteristic frequency of the input signal." Applicant respectfully submits that Hsu, Ghoshal, and Barrett do not disclose, either individually, or in any combination thereof, the foregoing.

Barrett does not even teach a phase lock loop.

Moreover, Ghoshal does not even disclose "an output signal with a desired characteristic frequency an integer, N, multiple of a characteristic frequency of an input signal." Applicants direct Examiner's attention to Ghoshal Figure 1 wherein the output clock 32 is illustrated. As can be seen from the Figure, the output clock 32 has the same frequency as the input signal, the equalized signal 24. Applicants also note that Ghoshal is directed to overcoming limitations in repeaters, see Ghoshal, column 1, which are by definition are not designed to provide "an output signal with a desired characteristic frequency an integer, N, multiple of a characteristic frequency of an input signal."

Examiner has indicated that Hsu teaches "a frequency divider circuit (M divider) for reducing the output frequency of a phase lock loop circuit." Office Action, at p. 3. However, the frequency divider in Hsu causes the frequency

gain to be _reduced_ by the factor, M, resulting in an output frequency that is N/M times the input frequency. See Hsu, Figure 1. In contrast, in Applicants' invention, the frequency gain between the output signal and the input signal is not reduced by the divider factor M.

If the teachings of Hsu were to be combined with Ghoshal, the resulting frequency of the phase lock loop circuit in Ghoshal would be reduced by the factor M. Hence the combination would not provide an output signal with a frequency that is N times the frequency of the input signal.

Accordingly, Applicants request allowance of independent claims 23 and 27 and dependent claims 24-26, and 28-30.

CLAIMS 31-37 ARE ALLOWABLE

Claim 31 is directed to a phase lock loop that provides "an output signal with a desired characteristic frequency an integer, N, multiple of a characteristic frequency of an input signal" that includes "a voltage controlled oscillator generating one or more oscillator signals, wherein each of the one or more signals are associated with M phases of the desired characteristic frequency of the output signal."

Applicants respectfully that Ghoshal, Hsu, or Barrett, either individually or in any combination, thereof do not teach the foregoing.

Barrett is not even directed to phase lock loop circuits. Hsu does not teach multi-phase signals. Although Examiner has indicated that "Ghoshal's figure 2 shows the timing reference generator is constructed to output multi-phase signals (58, 60, ... 68)", Office Action, 11/30/00, p. 2, Applicants respectfully submit that Ghoshal does not teach that the "signals are associated with M phases of the desired chracteristic frequency of the output signal."   There is no suggestion that any one of the signals in Ghoshal, figure 2, would be associated with M phases of the desired characteristic frequency of the output signal.

Moreover, as noted above, Ghoshal does not even disclose "an output signal with a desired characteristic frequency an integer, N, multiple of a characteristic frequency of an input signal."

Accordingly, Applicants request allowance of independent claim 31 and dependent claims 32-37.

CLAIM 38 IS ALLOWABLE

Claim 38 is directed to a phase lock loop comprising "a divider for reducing the oscillator frequency of the oscillator signal by an integer, M, factor thereby providing an output signal with the output frequency that is the integer, N, multiple of the input frequency" and "wherein the

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integer, N, is a factor for reducing the oscillator frequency to the frequency of the feedback signal."
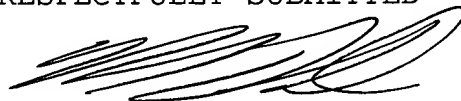
Applicants respectfully submit Ghoshal, Hsu, or Barrett, do not teach the foregoing, either individually or in any combination, thereof. As noted above, the frequency divider in Hsu causes the frequency gain to be _reduced_ by the factor, M, resulting in an output frequency that is N/M times the input frequency. As also noted above, Ghoshal does not even teach that the output frequency is a multiple of the input frequency, and Barrett does not even teach a phase lock loop.

Accordingly, Applicants request allowance of independent claim 38.

CONCLUSION

For the foregoing reasons, each of the pending claims 23-38 is allowable. Therefore, the application is in a condition for allowance and a notice of allowance is hereby requested.

RESPECTFULLY SUBMITTED

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